REMARKS

Claims 1-17 and 19-41 were pending in the application. By this paper, Applicant has amended Claims 1, 8, 14, 20, 25, 26, 34, 36 and 40, and add new Claims 42-45. Accordingly, Claims 1-17 and 19-45 are presented herein for examination.

Applicant files herewith a Request for Continued Examination (RCE) for further prosecution of the instant application.

General

Applicant thanks the Examiner for the detailed Office Action, which the Examiner clearly expended considerable effort preparing.

Drawing Objections

By this paper, Applicant has submitted a revised set of Figures substantively identical to those previously submitted, yet with the term "Replacement Sheet" included on each drawing pursuant to 37 C.F.R. 1.84(c).

Hence, Applicant submits that all objections to the drawings have been overcome.

Claim Objections and Rejections under §112

Claims 36-38 were rejected under 35 U.S.C. §112 second paragraph (see Pars. 5-8 of the Office Action). By this paper, Applicant has amended Claim 36 consistent with the Examiner's suggestions in Par. 8.

Accordingly, Applicant submits that these amendments overcome the Examiner's rejections.

Information Disclosure Statement (IDS)

Applicant submits herewith an IDS and PTO Form 1449 citing twenty (20) references for consideration by the Examiner.

Section 103 Rejections

Regarding the Examiner's Section 103 rejections of Claims 1-17 and 19-41 per Pars. 9-10 of the Office Action, Applicant provides the following responses.

Claim 1 - By this paper, Applicant has amended Claim 1 to include limitations relating to the recited digital processor having a mixed 16-bit and 32-bit instruction set architecture, and the recited method comprising providing a program having a plurality of different instruction types, including both 16-bit and 32-bit types. Support for these limitation are provided at, *inter alia*, page 11, lines 17-21 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 1 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 20 - By this paper, Applicant has amended Claim 20 to include limitations relating to the recited processor core being adapted to execute both 16-bit and 32-bit instructions without processor mode switching. Support for these limitation are provided at, *inter alia*, page 11, lines 17-21 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 20 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 26 - By this paper, Applicant has amended Claim 26 to include limitations relating to the recited method comprising providing a base instruction set having a plurality of 16-bit and 32-bit instructions. Support for these limitation are provided at, *inter alia*, page 11, lines 17-21 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited

by the Examiner cannot as a matter of law render Claim 26 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claim 40 - By this paper, Applicant has amended Claim 40 to include limitations relating to the recited method comprising providing an optimized instruction set comprising both 16-bit and 32-bit instructions. Support for these limitation are provided at, *inter alia*, page 11, lines 17-21 of Applicant's specification as filed.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 40 as amended obvious, since not every limitation of the claim is present or suggested in such art.

Claims 8, 14, 19, 25, 32, 34, 35 and 40 - By this paper, Applicant has amended Claims 8, 14, 25 and 40 to include limitations relating to the recited processor comprising a reduced instruction set computer (RISC). Support for these limitation are replete throughout Applicant's specification as filed. Claims 19, 32, 34 and 35 as previously presented already contain such limitations.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way, and in fact the Schlansker, et al, reference (U.S. 6,408,428) explicitly teaches away from Applicant's claimed inventions.

Specifically, Schlansker teaches a VLIW (very long instruction word) architecture and methods. Applicant respectfully traverses the Examiner's assertions that Schlansker in any way teaches or suggests a design process relating to a RISC processor. Claim 1 of Schlankser (reproduced in relevant part below) perhaps best encapsulates the intention of its invention:

> *1. A method for programmatic design of a VLIW processor comprising:*
>
> *reading a specification for at least one candidate VLIW processor, where the specification describes a specific instance of a parameterized VLIW processor design; ...*
>
> {emphasis added}

The Examiner's citations to, *inter alia*, Col. 16, line 38 of Schlansker (see page 20 of the Office Action, second paragraph, regarding Claim 19 rejection), refer to the design platform (e.g., workstation) on which the design process is conducted, and **not the target architecture**. For example, Col. 16 of Schlansker states:

> *"FIG. 1 is a block diagram illustrating the design flow in a VLIW design system. The system is implemented in collection of program modules written in the C.sup.++ programming language. While the system may be ported to a variety of computer architectures, the current implementation executes on a PA-RISC workstation or server running under the HP-UX 10.20 operating system."* {Emphasis added}

Hence, Schlansker does not teach that his methods/architecture for the target processor are in any way RISC-based or compatible therewith. This is so because as is well known to those of ordinary skill in the processor design arts, a VLIW architecture is at an architectural level completely different than a RISC processor. VLIW uses, *inter alia*, significant degrees of parallelism, many functional units, extremely long instructions words which are basically concatenations or composites of a plurality of smaller instruction words (hence the acronym "VLIW"), as well as typically a complete absence of branch prediction logic (VLIW processors typically perform all possible outcomes of the branch, and then decide which result to select afterwards).

Accordingly, Applicant submits that Schlansker (i) in no way teaches or suggests adaptation of its VLIW-specific approach to RISC; and (ii) pointedly teaches away from Applicant's claimed invention(s), since adaptation of his VLIW-specific apparatus and methods are completely incompatible with a RISC architecture such as that of Applicant's claimed invention(s).

Accordingly, the art cited by the Examiner cannot as a matter of law render Claims 8, 14, 19, 25, 32, 34, 35 and 40 as amended obvious, since not every limitation of these claims is present or suggested in such art.

Claim 34 - By this paper, Applicant has amended Claim 40 to include limitations relating to both the recited user-extension and configuration of the processor are performed as part of generating of a description language model of the processor. Support for these limitation are

provided at, *inter alia*, pages 20-22 of Applicant's specification as filed (see discussion of U.S. 6,862,563), and Fig. 33.

Applicant respectfully submits that none of the cited art used as the basis for the Examiner's rejection teaches or suggests such limitations in any way. Accordingly, the art cited by the Examiner cannot as a matter of law render Claim 34 as amended obvious, since not every limitation of the claim is present or suggested in such art. This is further buttressed by the independent basis for patentability for Claim 34 set forth previously herein

New Claims

By this paper, Applicant has added new Claims 42-45, each of which are supported by the specification as filed. See, *inter alia*, pages 20-22 of Applicant's specification as filed, and Fig. 33, as well as U.S. Patent No. 6,862,563 which was incorporated into the present application at time of filing thereof. Applicant submits that each of these new Claims distinguish over the art of record, and are also in condition for allowance.

Hence, in summary, Applicant submits that Claims 1-17 and 19-45 and are in condition for allowance. Applicant respectfully requests that the Examiner pass this case to issuance at the earliest opportunity.

Other Remarks

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

Furthermore, any remarks made with respect to a given claim or claims are limited solely to such claim or claims.

If the Examiner has any questions or comments that may be resolved over the telephone, he/she is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: April 18, 2005

By: _____

Robert F. Gazdzinski
Registration No. 39,990
11440 West Bernardo Court, Suite 375
San Diego, CA 92127
Telephone No.: (858) 675-1670
Facsimile No.: (858) 675-1674

ANNOTATED SHEET

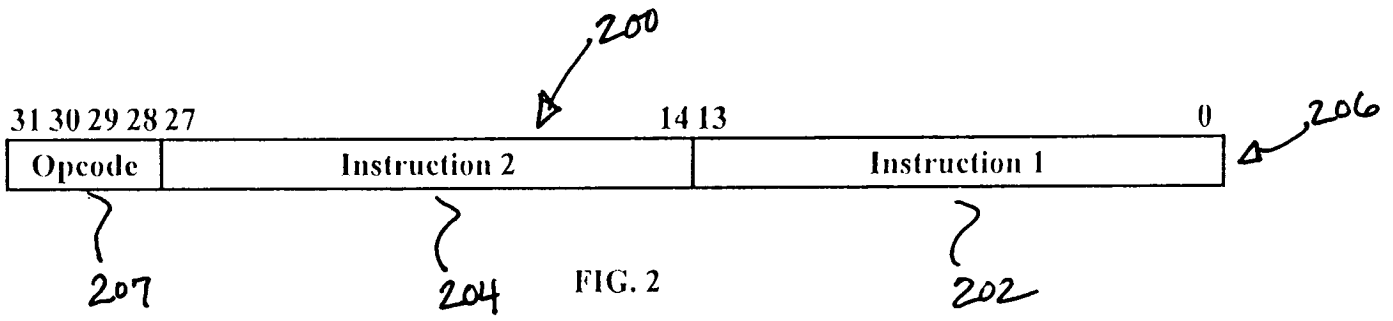

FIG. 2

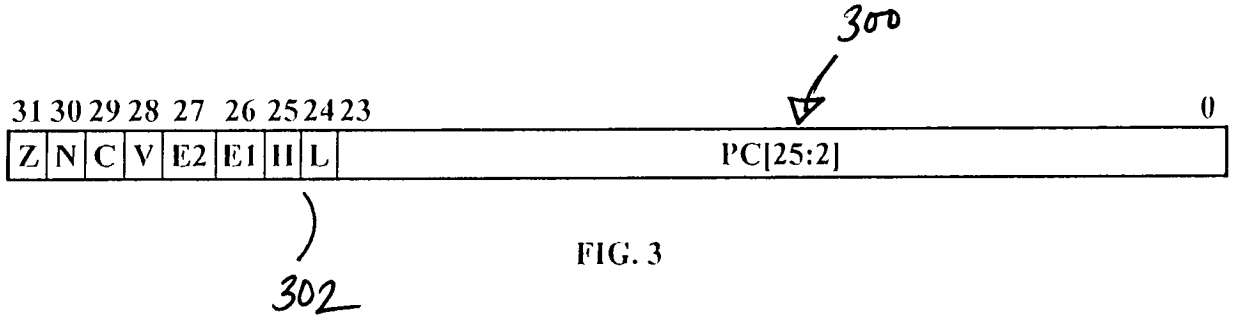

FIG. 3